CLAIMS

1. A semiconductor memory device comprising:

a silicon substrate including a gate and contact pads at both sides of the gate;

a second inter-insulation layer formed on the substrate, including a storage node contact and a bit-line contact, exposing a corresponding contact pad of the contact pads respectively, and including a bit-line pattern of a groove shape;

a storage node contact plug formed in the storage node contact; and

a damascene bit line, formed with the bit-line pattern, and connected with the exposed corresponding contact pad through the bit-line contact.

2. The semiconductor memory device according to claim 1, wherein the contact pad and the storage node contact plug comprise an epitaxial silicon layer.

3. The semiconductor memory device according to claim 1, wherein the contact pad and the storage node contact plug comprise a polysilicon layer.

4. The semiconductor memory device according to claim 1, wherein:

the gate is extended in a first direction, and the bit-line is extended in a second direction crossing the gate; and

a cross sectional length of a bottom of the storage node contact plug in the first direction and in the second direction are longer than a cross sectional length of the contact pad in the first direction and in the second direction.

5. The semiconductor memory device according to claim 4, wherein the bit-line comprises:

an insulation layer formed within the bit-line pattern;

a bit-line material filling within the bit-line pattern including the insulation layer; and

a capping layer formed on a top of the bit-line material within the bit-line pattern.

6. The semiconductor memory device according to claim 5, wherein the insulation layer functions as a bit-line spacer for insulating the bit-line and the storage node contact plug.

7. The semiconductor memory device according to claim 5, wherein the material of the insulation layer is different from the material of the capping layer, and a cross sectional length of the capping layer in the first direction is longer than a cross sectional length of the bit-line in the first direction.

8. The semiconductor memory device according to claim 7, wherein the capping layer comprises a nitride layer.

9. The semiconductor memory device according to claim 8, wherein the insulation layer is chosen from the group consisting of a thermal oxide layer and a high dielectric layer.

10. The semiconductor memory device according to claim 1, further comprising:

a first inter-insulation layer including self-aligned contacts exposing the silicon substrate at the both sides of the gate; and wherein

the gate has a stack structure comprising a gate insulation layer, a gate material, a capping layer, and a spacer in the sidewall thereof; and wherein the contact pads are formed in the self-aligned contacts.

11. The semiconductor memory device according to claim 1, further comprising:

an insulation layer formed on the bottom and the sidewall of the gate; and

a first inter-insulation layer formed on the silicon substrate and exposing the contact pads and the gate;

wherein the contact pads are formed on the silicon substrate and wherein the gate comprises a damascene type gate having a capping layer formed between the contact pads.

12. The semiconductor memory device according to claim 11, wherein:

a thickness difference between a portion of the insulation layer at a bottom of the gate and a portion of the insulation layer at a sidewall of the gate is within 7nm;

the portion of the insulation layer at the bottom of the gate comprises a gate insulation layer; and

the portion of the insulation layer at the sidewall of the gate comprises a gate spacer.

13. A fabrication method of a semiconductor memory device comprising the steps of:

providing a silicon substrate including a gate and contact pads;

forming a second inter-insulation layer on the silicon substrate;

etching the second inter-insulation layer to form a storage node contact exposing a corresponding contact pad;

forming a contact plug in the storage node contact that is connected to the corresponding contact pad;

etching the second inter-insulation layer to form a bit-line pattern with a groove shape;

etching the second inter-insulation layer to form a bit-line contact exposing the corresponding contact pad of the contact pads; and

forming a damascene bit-line within the bit-line pattern that is connected with the corresponding exposed contact pad through the bit-line contact.

14. The fabrication method of a semiconductor memory device according to claim 13, wherein the contact pad and the storage node contact plug comprise an epitaxially grown silicon layer.

15. The fabrication method of a semiconductor device according to claim 13, wherein the contact pad and the storage node contact plug comprise a polysilicon layer.

16. The fabrication method of a semiconductor memory device according to claim 13, wherein:

the gate is extended in a first direction, and the bit-line is extended in a second direction crossing the gate; and

a cross-sectional length of the bottom of the storage node contact in the first direction and in the second direction is longer than a cross-sectional length of the contact pad in the first direction and in the second direction, respectively.

17. The fabrication method of a semiconductor memory device according to claim 16, wherein forming a damascene bit-line further comprises:

forming an insulation layer formed within the bit-line pattern;

forming a bit-line material filling within the bit-line pattern including the insulation layer; and

forming a capping layer on a top of the bit-line.

18. The fabrication method of a semiconductor memory device according to claim 17, wherein forming the insulation layer comprises:

forming a bit-line spacer for insulating the bit-line and the storage node contact plug, the bit-line spacer chosen from the group consisting of an oxide layer and a high dielectric layer.

19. The fabrication method of claim 18, wherein forming the bit-line spacer comprises forming the bit line spacer using a process chosen from the group consisting of a thermal oxidation process and a deposition process.

20. The fabrication method of a semiconductor memory device according to claim 17, further comprising:

forming the capping layer from a material that is different from a material used for the insulation layer, and wherein a cross sectional length of the capping layer in the first direction is longer than a cross sectional length of the bit-line in the first direction.

21. The fabrication method of a semiconductor memory device according to claim 20, wherein forming the capping layer comprises:

etching back a portion of the insulation layer and the bit-line material within the bit-line pattern;

depositing a nitride layer on the silicon substrate; and

etching the nitride layer through a chemical mechanical polishing (CMP) process to form the capping layer.

22. The fabrication method of a semiconductor memory device according to claim 13, wherein providing the silicon substrate including the gate and the contact pads comprises:

forming a gate having a stack structure of a gate insulation layer, a gate insulation material, and a capping layer on the silicon substrate;

forming a spacer at the sidewall of the gate;

forming a first inter-insulation layer on the silicon substrate;

etching the first insulation layer to form self-aligned contacts exposing the silicon substrate at both sides of the gate; and

forming contact pads in the self-aligned contacts.

23. The fabrication method of a semiconductor memory device according to claim 13, wherein providing the silicon substrate including the gate and the contact pads comprises:

forming a sacrifice gate comprising a sacrifice gate insulation layer on the silicon substrate;

forming contact pads on the silicon substrate at both sides of the sacrifice gate;

forming a first inter-insulation layer on the silicon substrate to expose the contact pads and the sacrifice gate;

removing the exposed sacrifice gate to form an opening exposing the silicon substrate; and

forming the gate including an insulation layer in a bottom and a sidewall of the opening and a capping layer on the top thereof.

24. The fabrication method of a semiconductor memory device according to claim 23, wherein the insulation layer is chosen from the group consisting of a thermal oxide layer and a high dielectric layer; wherein a thickness difference between a portion of the insulation layer at a bottom of the gate and a portion of the insulation layer at a sidewall of the gate is within 7nm; wherein the portion of the insulation layer at the bottom of the gate comprises a gate insulation layer; and a portion of the insulation layer at the sidewall of the gate comprises a gate spacer isolating the gate from the contact pad.